JEFFREY COMPTON

(925) 212-7980 jeffrcompton@gmail.com

SUMMARY

Data driven engineer with strong communication skills and a hands-on approach. Experienced in a fast paced lean manufacturing environment with a track record of driving continuous improvement. Able to execute, prioritize and manage projects of varying scope and complexity. . Exposure to JMP, Mathematica, Matlab, C, assembly and python.

EXPERIENCE

Process Engineer **June 2011-June 2014**
Fairchild Semiconductor, South Portland, ME

Owned and maintained all process aspects of the RTP, ion implant and MEMS wafer bonding areas of the factory. Utilized SPC, DMAIC and other lean manufacturing principles to report results, systematically evaluate and improve manufacturing processes. Routinely consulted with stakeholders regarding technical approaches to projects and lead problem solving efforts individually and as part of cross-functional teams.

- Increased implant production capacity by 65%. Qualified 6 tools, including a unique platform
- Chosen to be owner of new, critical path MEMS bonding process transferred into the site
- Led a diverse team that resulted in a 35% cost avoidance of testing material after 6 months
- Developed first revs of silicon direct bond and eutectic bond processes
- Inspected, tested, accepted and owned EVG Gemini with Smart view NT system
- Eliminated 40% of post maintenance idle time and cut processing costs by re-engineering daily implant monitors
- Owned and updated FMEA documents for both area processes and specific technologies
- Monitored SPC charts on the tool, flow, and product level and adjusted process parameters to improve Cpk values, cycle time, yield and hold times
- Developed and improved reaction paths for out of control process controls
- Worked on multi-disciplinary integration teams, addressing technology specific yield loss
- Presented summaries of problem tools, process combinations and other factors contributing to yield and performance loss

Process Technology Development Engineer (co-op) **January 2011-June 2011**
Fairchild Semiconductor, South Portland, ME

Characterized process space and its impact on test results. Correlated in-line tests to reliability results of wafer level packaged products. Utilized visual failure modes and JMP for analysis

EDUCATION

M.S. in Applied Physics with Focus in PV/Semiconductors **2011**
University of Oregon, Materials Science Institute

B.S. in Physics with Emphasis in Earth Science **2008**
University of California, San Diego